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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,365	10/14/2004	Hendrik Klaas Jan Ten Dolle	NL 020324	8675

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
NGUYEN, HIEU P	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/511,365	TEN DOLLE ET AL.	
	Examiner	Art Unit	
	Hieu P. Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-5 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-5 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant is required to update the status (pending, allowed, etc.) of all parent priority applications in the first line of the specification. The status of all citations of US filed applications in the specification should also be updated where appropriate.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Sowlati (U.S. 6515547).

Regarding claim 1, Fig. 5A-5B of Sowlati discloses an amplifier circuit comprising input connections; a first and second current branch, each comprising an input transistor (M1/M3) and a cascode transistor (M2/M4), the input connections being coupled to control electrodes of the input transistors (M1/M3) in respective ones of the current branches, control electrodes of the cascode transistors (M2/M4) being coupled to each other as shown in Fig. 5B; a common current source circuit (inductor, Ls); output connections, each coupled to the common current source circuit via a series connection of the main current channels of the cascode transistor (M2/M4)

and the input transistor successively, of a respective one of the current branches; a high frequency coupling (capacitor Cb) between the control electrodes of the cascode transistors (M2/M4) and a node of the common current source arranged to copy substantially common mode voltage changes of terminals of the main current channels of the input transistors to voltage changes at the control electrodes of the cascode transistors.

Regarding claim 2, Sowlati discloses everything claimed as applied to claim 1. In addition, Sowlati further discloses in Fig. 5B an amplifier circuit, comprising a bias circuit (resistor(s), Rb) coupled to the control electrodes of the cascode transistors (M2/M4) for biasing the control electrodes of the cascode transistors. Since the claimed circuit is the same as the circuit of Sowlati, the bias circuit of Sowlati can be read as "a high frequency current blocking circuit" that blocks flow of current from the high frequency coupling through the biasing circuit.

Regarding claim 3, Sowlati discloses everything claimed as applied to claim 1. In addition, Sowlati further discloses in Fig. 5b an amplifier circuit, wherein the high frequency coupling comprises a capacitance (Cb) coupled between the control electrodes of the cascode transistors (M2/M4) and the node of the common current source, with a capacitance value so that common mode voltage changes of the terminals of the main current channels of the input transistors are substantially coupled to voltage changes at the control electrodes of the cascode transistors.

Regarding claim 4, Sowlati discloses everything claimed as applied to claim 1. In addition, Sowlati mentioned in col. 1, lines 7-9 the system is suitable for use in high- frequency application, thus meeting the claimed language of " a wide band high frequency signal distribution system" in claim 4.

Regarding claim 5, similar to claim 1, Sowlati discloses a structure as well as an method of amplifying a wide band signal the method comprising: inputting the wide band signal to a control electrode of input transistors (M1/M3) in a first and second current branch each current branch comprising one of the input transistors (e.g., M1 in Fig. 5b) and a cascode transistor (e.g., M2 in Fig. 5b) the input connections being coupled to control electrodes of the input transistors (M1/M3) in respective ones of the current branches control electrodes of the cascode transistors (M2/M4) being coupled to each other, outputting amplified signals from output connections that are coupled to a common current source circuit (Ls) via a series connection of the main current channels of the cascode transistor and the input transistor successively, of a respective one of the current branches; copying substantially common mode voltage changes of terminals of the main current channels of the input transistors to voltage changes at the control electrodes of the cascode transistors, at least in a frequency band of the wide band signal.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hieu Nguyen whose telephone number is 571-272-8577. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hieu Nguyen
AU: 2817

hn

Robert Pascal
Primary Examiner

Supervisory Patent Examiner
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